REMARKS

This amendment is in response to the Office Action dated March 24, 2004. A petition for a two-month extension of time is also enclosed. Entry of this Amendment and reconsideration of this application are respectfully requested.

Claim Rejections under 35 USC 103(a)

Claims 1-19 were rejected as obvious over a patent to Shigematsu et al. in combination with a patent to Hébert.

Claim 1

Claim 1 has been amended to better clarify its distinctions with respect to the cited art. As amended, claim 1 is directed to a specific bipolar junction transistor (BJT) structure. The recited structure is dependent on certain characteristics of the fabrication process used to make the transistor, specifically its minimum process dimension - identified in the claim as "X μm" - and its minimum alignment tolerance.

The claimed structure requires:

- a semi-insulating substrate,
- a subcollector formed on the substrate,
- a collector formed on the subcollector,
- a first metal contact on the subcollector which provides a collector contact for the BJT,
- a base formed on the collector,
- an emitter formed on the base,
- a cross-shaped second metal contact on the emitter which provides an emitter contact for the BJT, the emitter contact comprising two perpendicular arms which intersect at a central

area, the width of each of the arms being about equal to X μm;
- an inter-level dielectric layer on the emitter contact; and
- a via through the inter-level dielectric layer which provides access to the emitter contact, the via being square-shaped, centered over the center point of the central area, and oriented at a 45° angle to the arms such that the via can be sized as large as possible while maintaining the minimum alignment tolerance with respect to the boundaries of the emitter contact.

The structure recited in the amended claim 1 provides specific and novel solutions to specific BJT fabrication problems. The applicant is concerned with the base resistance (R_B) and base-collector capacitance (C_{BC}) that arise due to the width of a BJT device's emitter fingers, and to the connection method used to contact the emitter. Higher R_B and C_{BC} values tend to degrade a BJT's RF performance. To reduce these values, the applicants devised a structural approach which enables the width of each emitter finger to be made as narrow as allowed by the device's fabrication process, and contact to be made to the emitter fingers without any appreciable increase in capacitance or resistance.

The applicants' approach includes two primary components: an emitter contact having very specific characteristics, and the use of an inter-level dielectric layer and a specific via design to effect a connection to that contact.

Emitter contact

Claim 1 requires that the emitter be formed on the base, and that "a cross-shaped second metal contact" be formed on the emitter which provides an emitter contact for the BJT. The emitter contact comprises "two perpendicular arms which intersect at a central area, the width of each of said arms being about

equal to X μm". This language establishes that the emitter contact is in the shape of a cross, with the width of each arm being made about equal to X μm - i.e., the narrowest possible width allowed for the particular fabrication process used to make the device. As explained on page 4 at line 31:

"Making the arms of emitter contact 24 as narrow as possible reduces base resistance (R_B) and base-collector capacitance (C_{BC}), and thus improves RF performance. In addition, the contact's cross shape allows a uniform current distribution path, providing better heat spreading and hence higher device reliability."

Inter-level dielectric layer and via

As presently amended, claim 1 requires that there be an "inter-level dielectric layer on said emitter contact", and a "via through said inter-level dielectric layer which provides access to said emitter contact, said via being square-shaped, centered over the center point of said central area, and oriented at a 45° angle to said arms such that said via can be sized as large as possible while maintaining said minimum alignment tolerance with respect to the boundaries of said emitter contact." That is, when the via is shaped and oriented in the specific manner required by claim 1, connection to the emitter contact is made from above - probe-like - with the largest possible contact that still meets the minimum alignment tolerance, thereby enabling a low capacitance, low resistance connection.

This combination of structural requirements provides a number of advantages. As explained on page 4 at line 11, the required emitter contact design, inter-level dielectric layer, and via design:

". . . allows via 30 to be as large as possible while the width of emitter contact arms 32 and 34 is as narrow as possible. Thus, if the minimum dimension for the process used to fabricate the device is 0.6 μm, and the alignment tolerance is 0.3 μm, the width of each of emitter contact arms 32 and 34 can be made equal to 0.6 μm. Then, because via 30 is oriented at a 45° angle to the arms, the via size can be 0.6μm x 0.6μm or larger (0.71μm x 0.71μm in this example) and still maintain the 0.3 μm alignment tolerance."

The narrow emitter contact arms serve to keep base resistance (R_B) and base-collector capacitance (C_{BC}) as low as allowed by the device's fabrication process, while the inter-level dielectric layer and via enable connection to the emitter contact without any appreciable increase in capacitance or resistance. These structural features serve to reduce extrinsic parasitics while increasing high frequency limits, thereby making the invention particular well-suited to millimeter wave operation with devices such as InP-based HBTs (though the invention is in no way limited to use with InP-based devices).

The cited art is quite different. The patent to Shigematsu describes a method to fabricate InP-based HBTs. It is very specific to the InP-based system and is dependent on one central idea: that the extrinsic base resistance can be reduced by the regrowth of a very heavily doped second base layer of InGaAsSb which is grown halfway through the process on the exposed thin base layer (InGaAsSb), or on the top of the collector layer. Separation of the base and emitter outside the intrinsic junction are dependent on a thin silicon nitride layer placed on the emitter mesa wall prior to the regrowth.

Shigematsu says <u>nothing</u> about emitter contact shape, process

dimensions, inter-level dielectric layers, or vias - all of which are central to the structure recited in claim 1, and to the essence of the applicants' invention. In fact, Shigematsu fails to disclose or suggest any of the following elements of the amended claim 1:

- a cross-shaped metal contact on the emitter comprising two perpendicular arms which intersect at a central area, the width of each of the arms being about equal to X μm;
- an inter-level dielectric layer on the emitter contact; and
- a square-shaped via through the inter-level dielectric layer which provides access to the emitter contact, centered over the center point of the central area and oriented at a 45° angle to the arms such that the via can be sized as large as possible while maintaining the minimum alignment tolerance with respect to the boundaries of the emitter contact.

The Examiner looks to Hébert to overcome the shortcomings of the patent to Shigematsu. It fails to do so. The Hébert patent explores ways to reduce base-to-collector capacitance by minimizing the base 'diffusion', i.e. the base-collector junction area. To do this, Hébert speculates on different emitter configurations, always focusing on reducing the area of the base diffusion - often at the expense of increasing base resistance. In the course of this exploration, Hébert mentions the possibility of using an emitter shaped as a cross, as well as several other shapes. Throughout Hébert's discussion of the emitter-base layouts, his method of contacting the emitter (and base) is the usual surface overlayer of metal which must be routed in a complicated manner not consistent with high frequency performance (because of added capacitance and resistance).

It should also be noted that Hébert never discloses or suggests a cross-shaped emitter contact having arms with the narrowest possible width permitted by the fabrication process. On the contrary, when citing examples of various possible emitter configurations at column 4, line 30, he lists "a so-called "lozenge" structure, for relatively narrow emitters, a "cross" structure for wider emitters, and a "T" structure". This is because his use of a cross-shaped emitter is solely based on the possibility of it allowing a smaller intrinsic device area (base diffusion area). Thus, Hébert actually teaches away from a structure which provides the narrowest possible emitter contact, which is explicitly required by the applicants' claim 1.

Hébert also fails to disclose or suggest the specific inter-level dielectric layer, square-shaped via, via orientation, and via sizing requirements recited in claim 1 - instead disclosing only a conventional surface overlayer of metal. The applicants' requirement of an inter-layer dielectric layer and novel via arrangement at the center of the narrowest-possible cross-shaped emitter contact enables very low capacitance "probe-like" connection to the device's emitter, base and collector. The use of the cross-shaped emitter contact allows access to four emitter fingers without any appreciable increase in capacitance or resistance, which is contrary to Hébert's approach. Thus, the low resistance/low capacitance advantages gained by the applicants' via approach are not and cannot be achieved with Hébert's design.

To summarize, Hébert fails to disclose or suggest any of the following elements of the amended claim 1:

- a cross-shaped metal contact for which the width of each of the arms is about equal to X μm;

- an inter-level dielectric layer on the emitter contact; and
- a square-shaped via through the inter-level dielectric layer which provides access to the emitter contact, centered over the center point of the central area and oriented at a 45° angle to the arms such that the via can be sized as large as possible while maintaining the minimum alignment tolerance with respect to the boundaries of the emitter contact.

Hébert and Shigematsu fail to disclose numerous essential elements of the amended claim 1. Therefore, under close analysis, it is seen that, even if combined as suggested by the Examiner, Shigematsu and Hébert fail to disclose the invention recited in the amended claim 1. If fact, if anything, that which is disclosed by the combined references actually teaches away from that which is claimed by the applicants as their invention.

The applicants assert that, in light of these facts, those of "ordinary skill in the art" in this field could not have moved from the ideas of Hébert and Shigematsu to the devices described in the amended claim 1. For all of the reasons noted above, the amended claim 1 would not have been obvious in view of the cited art at the time the invention was made. The amended claim is thus allowable over Hébert and Shigematsu.

Claims 2-11

The amended claim 1 is the parent of each of claims 2-11, which should thus also be allowable. Note that, as the limitation formerly found in claim 2 has been added to claim 1, claim 2 has been cancelled.

Claim 12

Claim 12 is similar in scope to the amended claim 1, except

that it is specifically directed to a heterojunction bipolar transistor (HBT). As with claim 1, the structure recited in claim 12 is dependent on the HBT's fabrication process - specifically its minimum process dimension "X μm", and its minimum alignment tolerance. Claim 12 requires:

- a semi-insulating substrate comprising a compound semiconductor;
- a subcollector formed on the substrate;
- a collector formed on the subcollector;
- a first metal contact on the subcollector which provides a collector contact for the HBT;
- a base formed on the collector;
- an emitter formed on the base;
- a cross-shaped second metal contact on the emitter which provides an emitter contact for the BJT, the emitter contact comprising two perpendicular arms which intersect at a central area, the width of each of the arms being about equal to X μm;
- an inter-level dielectric layer on the emitter contact; and
- a via through the inter-level dielectric layer which provides access to the emitter contact, the via being square-shaped, centered over the center point of the central area, and oriented at a 45° angle to the arms, the square-shaped via sized as large as possible while maintaining the minimum alignment tolerance with respect to the boundaries of the emitter contact.

The approach recited in claim 12 requires an emitter contact having very specific characteristics, and the use of an inter-level dielectric layer and a specific via design to effect a connection to that contact. The emitter contact is cross-shaped, with arms having a width about equal to X μm - i.e., the narrowest possible width allowed for the particular fabrication

process used to make the device. This reduces base resistance (R_B) and base-collector capacitance (C_{BC}), and thus improves RF performance. In addition, the contact's cross shape allows a uniform current distribution path, providing better heat spreading and hence higher device reliability.

Claim 12 also requires that there be an inter-level dielectric layer, and a square-shaped via through the dielectric layer which is centered over the center point of the central area and oriented at a 45° angle to the arms. The claim also requires that the via be sized as large as possible while maintaining the minimum alignment tolerance with respect to the boundaries of the emitter contact. This combination of structural requirements provides a number of performance advantages, such as reduced extrinsic parasitics and increased high frequency limits. These advantages are particular valuable when employed with a transistor designed for use at high speeds, such as a HBT.

As noted above, the cited art fails to disclose many of the essential elements of claim 12. Shigematsu describes a method to fabricate InP-based HBTs, the extrinsic base resistance of which can be reduced by the regrowth of a very heavily doped second base layer of InGaAsSb which is grown halfway through the process on the exposed thin base layer (InGaAsSb), or on the top of the collector layer. Shigematsu does <u>not</u> discuss emitter contact shape, process dimensions, inter-layer dielectric layers, or via designs at all - just how to use regrowth to reduce base resistance. In fact, Shigematsu fails to disclose or suggest <u>any</u> of the following elements of the amended claim 1:

- a cross-shaped metal contact on the emitter comprising two perpendicular arms which intersect at a central area, the width

of each of the arms being about equal to X μm;

- an inter-level dielectric layer on the emitter contact; and

- a square-shaped via through the inter-level dielectric layer which provides access to the emitter contact, centered over the center point of the central area and oriented at a 45° angle to the arms, the square-shaped via sized as large as possible while maintaining the minimum alignment tolerance with respect to the boundaries of the emitter contact.

The Examiner again looks to Hébert to overcome the shortcomings of the patent to Shigematsu, but again it fails to do so.

The Hébert patent explores ways to reduce base-to-collector capacitance by minimizing the base 'diffusion', i.e. the base-collector junction area. To do this, Hébert speculates on different emitter configurations, always focusing on reducing the area of the base diffusion - often at the expense of <u>increasing</u> base resistance. Throughout Hébert's discussion of the emitter-base layouts, his method of contacting the emitter (and base) is the usual surface overlayer of metal which must be routed in a complicated manner not consistent with high frequency performance (because of added capacitance and resistance).

Hébert never discloses or suggests a cross-shaped emitter contact having arms with the narrowest possible width permitted by the fabrication process. On the contrary, when citing examples of various possible emitter configurations, he recommends the use of a "cross" structure for <u>wider emitters</u>. That is, Hébert actually <u>teaches away</u> from a structure which provides the narrowest possible emitter contact, which is explicitly required by the applicants' claim 12.

And, as noted above, Hébert also fails to disclose or

suggest the specific inter-level dielectric layer, square-shaped via, via orientation, and via sizing requirements recited in claim 12 - instead disclosing only a conventional surface overlayer of metal.

To summarize, Hébert fails to disclose or suggest any of the following elements of claim 12:

- a cross-shaped metal contact for which the width of each of the arms is about equal to X μm;
- an inter-level dielectric layer on the emitter contact; and
- a square-shaped via through the inter-level dielectric layer which provides access to the emitter contact, centered over the center point of the central area and oriented at a 45° angle to the arms, the square-shaped via sized as large as possible while maintaining the minimum alignment tolerance with respect to the boundaries of the emitter contact.

Therefore, even if combined as suggested by the Examiner, the combination of Shigematsu and Hébert fails to disclose or suggest the invention recited in claim 12, as Hébert and Shigematsu lack disclosure of numerous essential elements of claim 12. For all of the reasons noted above, the applicants assert that claim 12 would not have been obvious in view of the cited art at the time the invention was made. Claim 12 is thus allowable over Hébert and Shigematsu.

Claims 13-19

Claim 12 is the parent of each of claims 13-19, which should thus also be allowable.

All of the claims presently in the application are believed to be patentably distinct with respect to the cited art and to otherwise be in proper form for allowance. A Notice of Allowance is respectfully requested.

Respectfully submitted,

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